

FIG. 2 is a block diagram of a clock distribution system 20 in accordance with the prior art. The system 20 includes a phase-locked loop (PLL) 15, a clock driver 17, a clock network 19, and a clock receiver 22. The PLL 15 is configured to receive a reference clock (ref_clk) and generate a chip clock (chip_clk). The chip_clk is distributed to the clock driver 17, which drives the clock network 19. The clock network 19 is a mesh of horizontal and vertical lines, with diagonal lines representing parasitic capacitance. The clock network 19 is connected to the clock receiver 22, which includes a Latch 22 and a Flip-Flop 28. The clock receiver 22 is configured to receive the clock signal from the clock network 19 and provide a clock signal to the Flip-Flop 28. The clock receiver 22 is also connected to a feedback loop 26, which provides a feedback signal to the PLL 15. The clock receiver 22 is also connected to a clock driver 17, which drives the clock network 19. The clock driver 17 is configured to receive the chip_clk from the PLL 15 and drive the clock network 19. The clock network 19 is a mesh of horizontal and vertical lines, with diagonal lines representing parasitic capacitance. The clock network 19 is connected to the clock receiver 22, which includes a Latch 22 and a Flip-Flop 28. The clock receiver 22 is configured to receive the clock signal from the clock network 19 and provide a clock signal to the Flip-Flop 28. The clock receiver 22 is also connected to a feedback loop 26, which provides a feedback signal to the PLL 15.

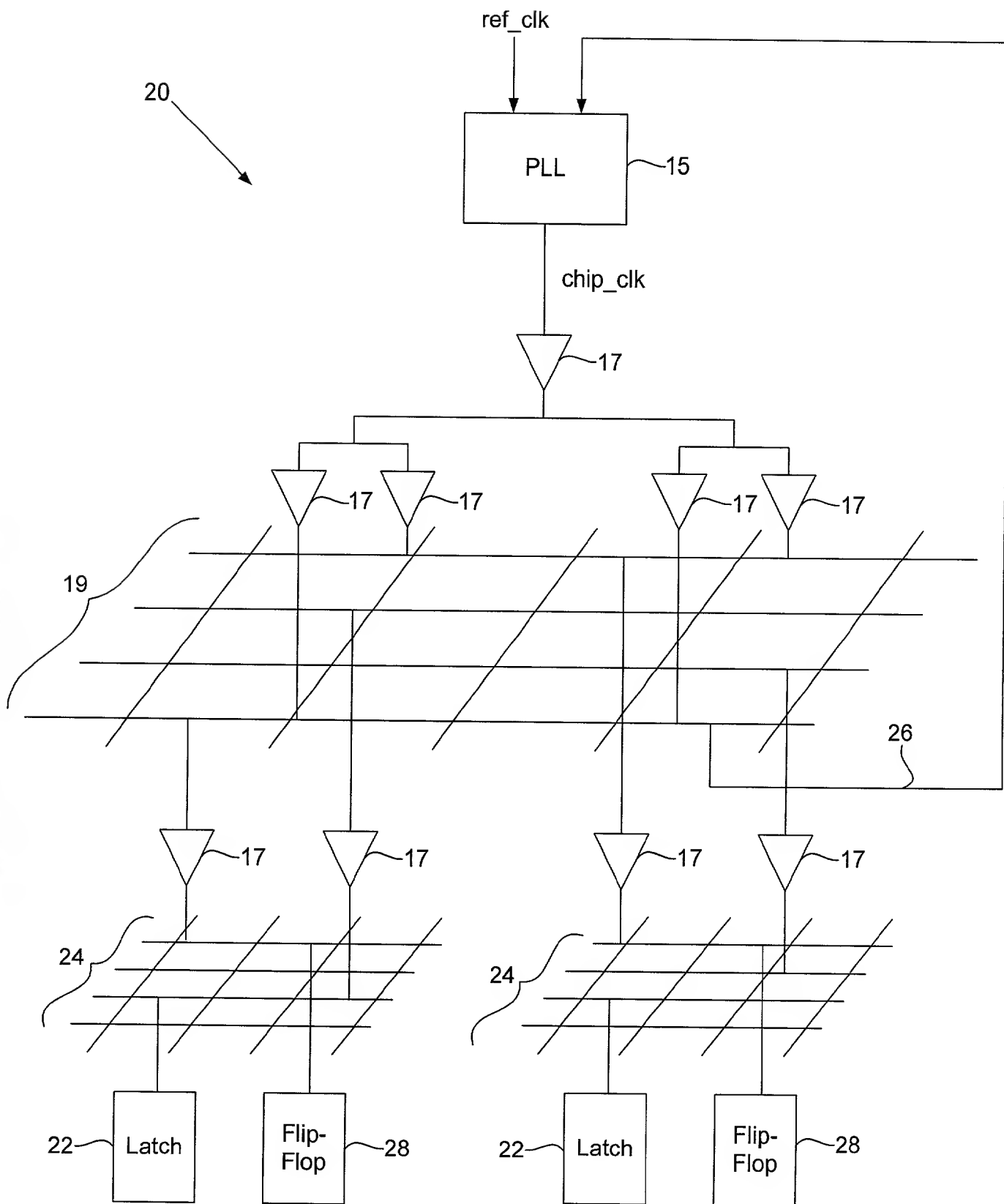


FIGURE 2
(Prior Art)

FIG. 3a is a schematic diagram of a grid structure 42. The grid structure 42 is bounded by two horizontal bars 40. A dashed circle indicates a magnified view of a portion of the grid structure 42, which is shown in FIG. 3b.

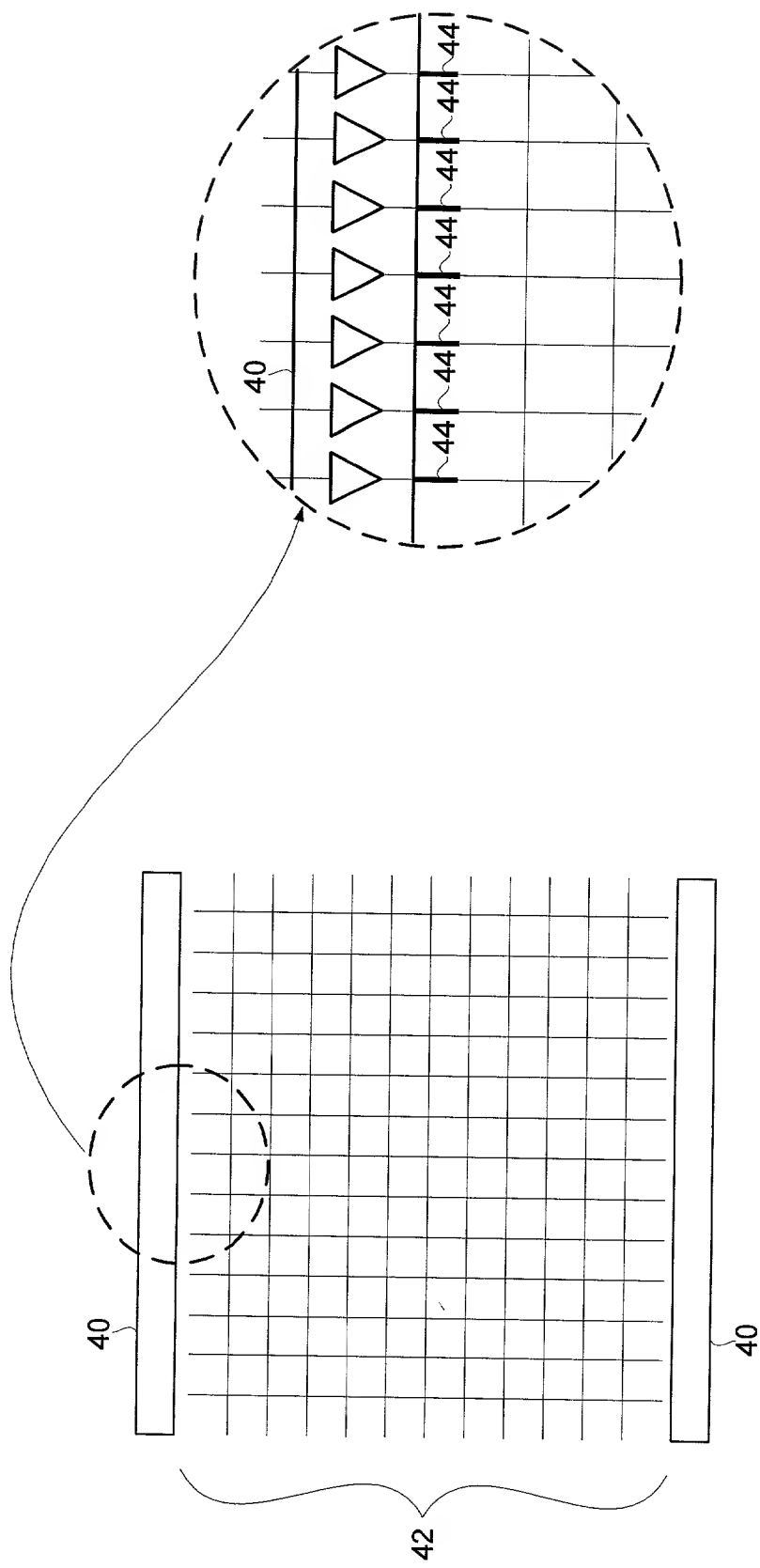


FIGURE 3a
(Prior Art)

FIGURE 3b
(Prior Art)

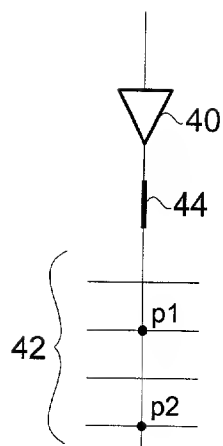


FIGURE 3c
(Prior Art)

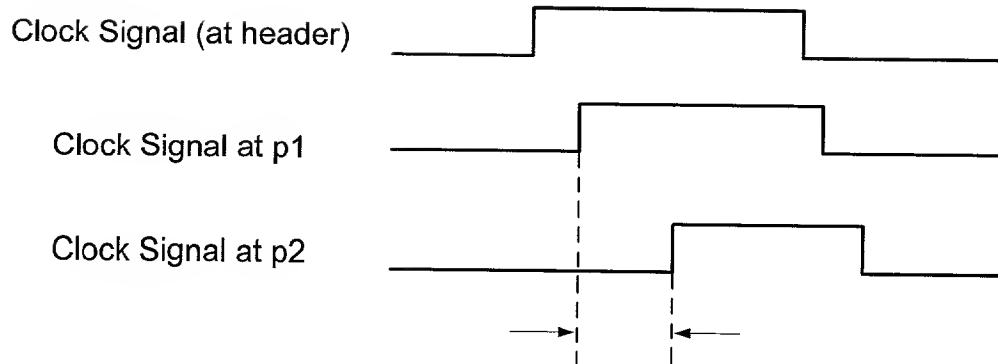


FIGURE 3d
(Prior Art)

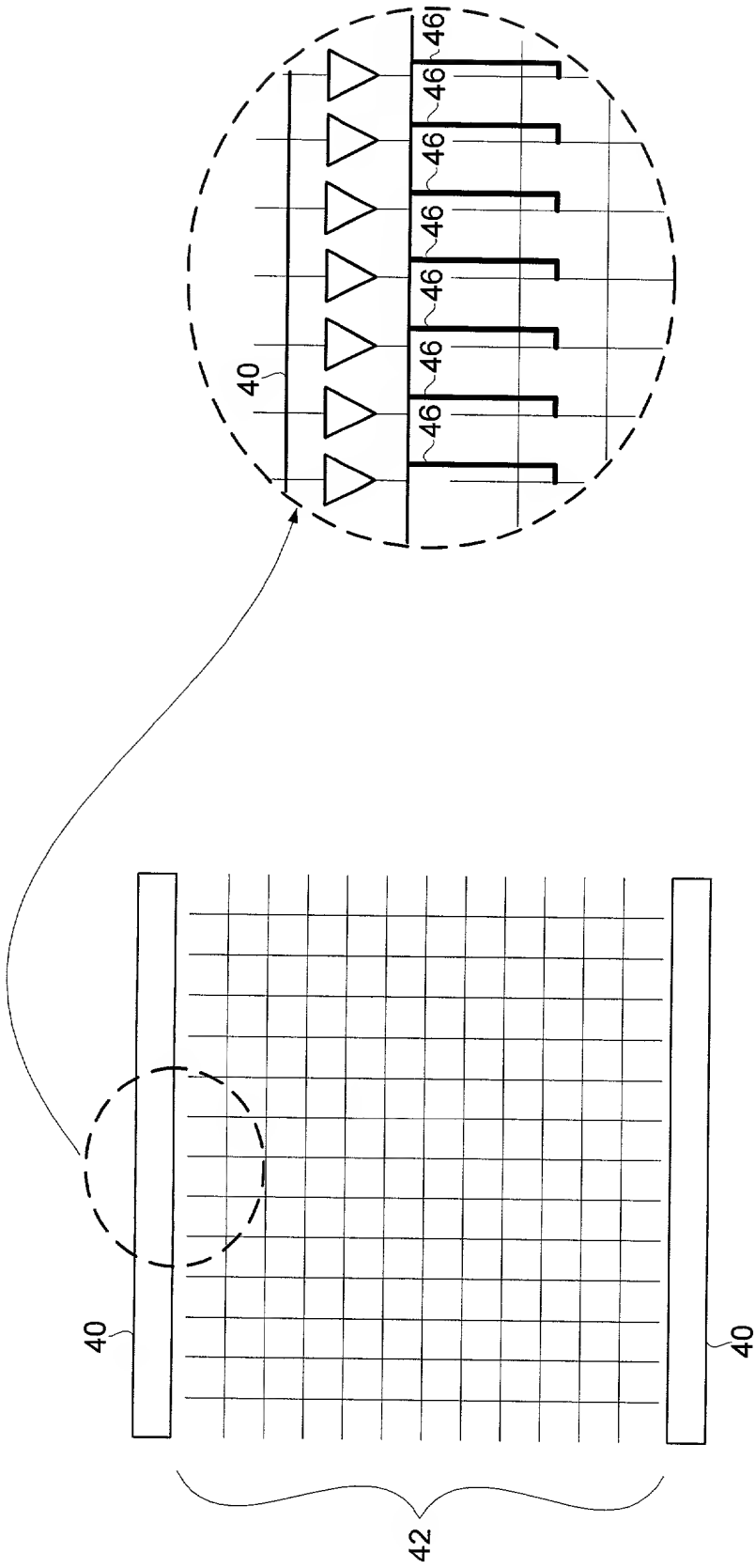


FIGURE 4a

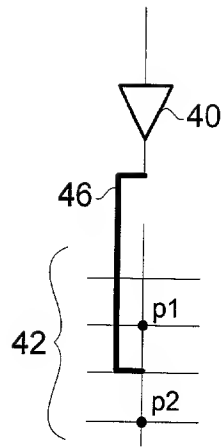


FIGURE 4b

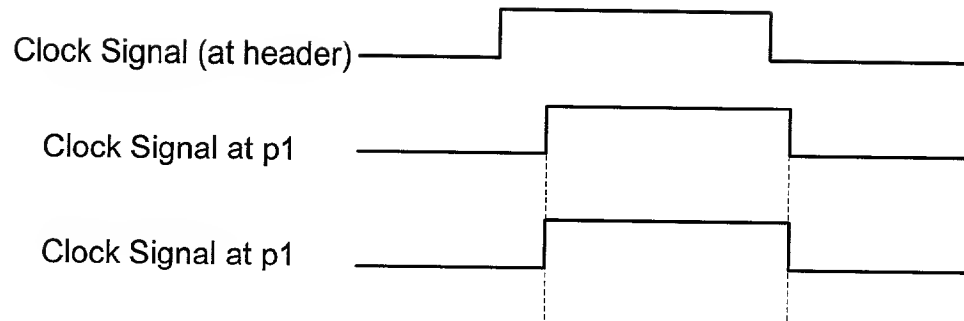


FIGURE 4c

FIG. 5 is a schematic diagram of a circuit 40, which is a part of a system 10, for controlling a motor 12. The circuit 40 includes a microcontroller 42, a motor 12, and a power supply 44. The microcontroller 42 is connected to the motor 12 and the power supply 44. The power supply 44 is connected to the motor 12. The microcontroller 42 is connected to the motor 12. The power supply 44 is connected to the motor 12.

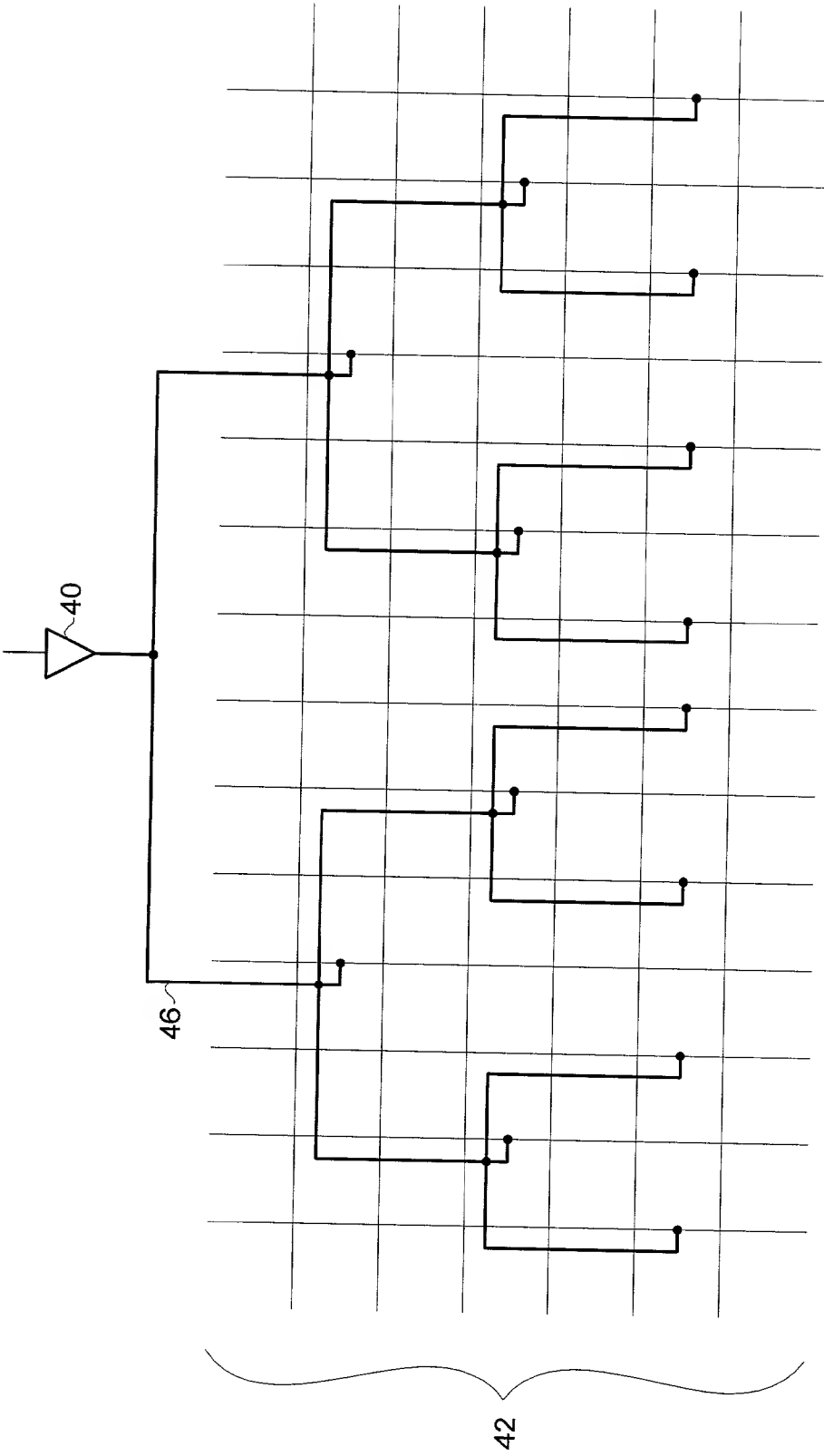


FIGURE 5